Jeehwan Kim

Associate Professor of Mechanical Engineering
Associate Professor of Materials Science and Engineering

Massachusetts Institute of Technology

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Research Projects

Neuromorphic computing	- 1R-based ANN arrays for online training/inference (NSF) - Artificial synapses based on single-crystalline ReRAM (SRC)
Remote epitaxy, **Graphene-based layer transfer**	- III-V/III-N MicroLEDs - Freestanding InGaAs-based IR Photodectors (LG) - Freestanding Multifunctional complex oxides for magnetoelectriccoupling (DARPA) - SiC/IIII-N power electronics (ROHM, Analog Device)
Renewable energy, **Energy storage**	- Wafer recycling technique for GaAs solar cells based on remote epitaxy (DOE) - High efficiency III-V multi-junction solar cells based on remote epitaxy (AFRL) - Single-crystalline all solid-state battery (Hyundai Motors)
Heterointegration, **Flexible electronics**	- Skin strain sensor arrays (Amore Pacific) - Flexible/transparent microLEDs - Self-powered IoT system
Two-dimensional materials	- Wafer-scale single-crystalline 2D materials - Wafer-scale 2D heterostructures

Education

Ph.D.	Materials Science and Engineering	University of California at Los Angeles, CA, USA	2008
M.S.	Materials Science and Engineering	Seoul National University, Seoul, Korea	1999
B.S.	Materials Science and Engineering	Hongik University, Seoul, Korea	1997

Work Experience

Massachusetts Institute of Technology, *Cambridge, MA* Department of Materials Science and Engineering Department of Mechanical Engineering	Associate Professor	2018 – date
Massachusetts Institute of Technology, *Cambridge, MA* Department of Materials Science and Engineering Department of Mechanical Engineering	Assistant Professor	2016 – 2018
IBM T.J. Watson Research Center, *Yorktown Heights, NY* Department of Silicon Technology	Research Staff Member	2008 – 2015
IBM T.J. Watson Research Center, *Yorktown Heights, NY* Department of Silicon Technology	Research Intern	2007
Korea Air Force, *Suwon, Korea*	Airman First Class	1999 – 2002

Teaching Experience

2.671 Instrument and Measurement 2017
Massachusetts Institute of Technology, MA
2.674 Micro-Nano Engineering Laboratory 2016
Massachusetts Institute of Technology, MA
2.001 Mechanics & Materials 2015
Massachusetts Institute of Technology, MA
MSE 104, Introduction to Materials Science 2005 – 2006
University of California at Los Angeles, CA

Awards

IBM Faculty Award 2016
IBM Corporation
Lam Research Foundation Grant 2016
LAM Research
Master Inventor of IBM Corporation 2012
IBM
High Value Patent Application Awards (10 times) 2011 – 2015
IBM
Invention Achievement Awards (23 times) 2009 – 2015
IBM

Professional Activities

Technical Committee/Chair
Organizer of Compound Semiconductor Week 2018, IEEE Electron Device Society, The International Conference on Silicon Epitaxy and Hetero-structures, The International Society for Optics and Photonics
Journal referee
Nature, Nature Communications, Science Advances, Advanced Materials, ACS Nano, Scientific Reports, Small, Nanoscale, Applied Physics Letters, Journal of Materials Chemistry A, IEEE Electron Device Letters, IEEE transactions on Nanotechnologies, Journal of Electrochemical Society, Organic Electronics

Articles Featuring Prof. Kim's Research Achievement

CNBC News article: MIT researchers develop new chip design to take us closer to computers that work like human brains
https://www.cnbc.com/2018/10/08/mit-develops-a-chip-to-help-computers-work-more-like-human-brains-.html
Nature News & Views: Transparency revealed
https://www.nature.com/articles/s41563-018-0201-7
MIT News: Researchers quickly harvest 2-D materials, bringing them closer to commercialization
http://news.mit.edu/2018/researchers-quickly-harvest-single-atom-materials-1011
Nature News & Views: Tightening grip
https://www.nature.com/articles/s41563-018-0020-x
MIT News: Engineers design artificial synapse for "brain-on-a-chip" hardware
http://news.mit.edu/2018/engineers-design-artificial-synapse-brain-on-a-chip-hardware-0122
The Verge: MIT researchers say new chip design takes us closer to computers that work like our brains
https://www.theverge.com/2018/1/24/16927040/ai-neuromorphic-engineering-computing-mit-brain-chip
Nature News & Views: Materials Science: Crystals align through graphene
http://www.nature.com/nature/journal/v544/n7650/full/544301a.html
MIT News: Not stuck on silicon
http://news.mit.edu/2017/graphene-copy-machine-cheaper-semiconductor-wafers-0419
EETimes: New Method Cuts Cost of GaAs Circuits
http://www.eetimes.com/document.asp?doc_id=1331617
IEEE Spectrum: Graphene Makes Infinite Copies of Compound Semiconductor Wafers

http://spectrum.ieee.org/nanoclast/semiconductors/materials/graphene-makes-infinite-copies-of-exotic-semiconductor-wafers
MIT News: Researchers "iron out" graphene
http://news.mit.edu/2017/iron-out-graphene-wrinkles-conductive-wafers-0403
EETimes: IBM Conquers Wafer-Scale Graphene
http://www.eetimes.com/document.asp?doc_id=1324128
IBM Research News: First wafer-scale single-crystalline monolayer graphene
http://ibmresearchnews.blogspot.com/2013/11/exfoliating-wafer-scale-graphene-down.html#fbid=Ramw25RHxOc
IBM Research News: Growing single-crystalline materials on reusable graphene
http://ibmresearchnews.blogspot.com/2014/09/growing-single-crystalline-materials-on.html
EETimes Europe: GaN for analog boosted by IBM tape lift-off
http://www.electronics-eetimes.com/en/gan-for-analog-boosted-by-ibm-tape-lift-off.html?cmp_id=7&news_id=222922628&page=2
Electronics Weekly: Will 2015 be the key year for graphene?
http://www.electronicsweekly.com/news/research/materials-rd/will-2015-key-year-graphene-2015-01/

List of Publications

Journal Papers (Corresponding authors)

1. Jaewoo Shim, Sang-Hoon Bae, Wei Kong, Doyoon Lee, Kuan Qiao, Daniel Nezich, Yong Ju Park, Ruike Zhao, Suresh Sundaram, Xin Li, Hanwool Yeon, Chanyeol Choi, Hyun Kum, Ruoyu Yue, Guanyu Zhou, Yunbo Ou, Kyusang Lee, Jagadeesh Moodera, Xuanhe Zhao, Jong-Hyun Ahn, Christopher Hinkle, Abdallah Ougazzaden, and **Jeehwan Kim*,**
   "Controlled crack propagation for atomic precision handling of wafer-scale two-dimensional materials"
   Science online (2018)

2. Wei Kong, Huashan Li, Kuan Qiao, Yunjo Kim, Kyusang Lee, Tom Osadchy, Richard J Molnar, D. Kurt Gaskill, Rachael L. Myers-Ward, Kevin M. Daniels, Yuewei Zhang, Suresh Sundram, Yang Yu, Sang-hoon Bae, Siddharth Rajan, Yang Shao-Horn, Abdallah Ougazzaden, Jeffrey C. Grossman*, and **Jeehwan Kim***
   "Polarity governs atomic interaction through two-dimensional materials"
   Nature Materials online (2018)

3. Shinhyun Choi, Scott Tan, Yunjo Kim, Chanyeol Choi, Pai-Yu Chen, and Shimeng Yu, and **Jeehwan Kim***,
   "SiGe Epitaxial Memory for Neuromorphic Computing with reproducible high performance based on engineered dislocations",
   Nature Materials, Vol. 17, 335–340 (2018) *Featured as a table of content cover*

4. Yunjo Kim, Samuel S. Cruz, Kyusang Lee, Babatunde O. Alawode, Chanyeol Choi, Yi Song, Jared M. Johnson, Chris Heidelberger, Wei Kong, Shinhyun Choi, Kuan Qiao, Eugene A. Fitzgerald, Jing Kong, Alexie M. Kolpak, Jinwoo Hwang, and **Jeehwan Kim***,
   "Remote epitaxy through graphene enables two-dimensional material-based layer transfer"
   Nature, Vol. 544, 340–343 (2017) *Featured as a front cover*

5. Sang-Hoon Bae, Xiaodong Zhou, Seyoung Kim, Yun Seog Lee, Samuel Cruz, Yunjo Kim, James B. Hannon, Yang Yang, Devendra K. Sadana, Frances M. Ross, Hongsik Park, and **Jeehwan Kim***
   "Unveiling the carrier transport mechanism in epitaxial graphene for forming wafer-scale, single-domain graphene",
   Proceedings of the National Academy of Science, Vol. 114, 4082-4086 (2017)

6. Talia Gershon, Yun Seog Lee, Teodor K. Todorov, Wei Wang, Mark T. Winkler, Marinus Hopstaken,Oki Gunawan, **Jeehwan Kim***
   "Atomic layer deposited aluminum oxide for interface passivation of $Cu_2ZnSn(S,Se)_4$ thin-film solar cells
   Advanced Energy Materials, 1600198 (2016)

7. **Jeehwan Kim*,** Ziruo Hong*, Gang Li, Tze-bin Song, Jay Chey, Devendra Sadana, and Yang Yang*, "10.5% amorphous silicon/polymer tandem photovoltaic cell", ***Nature Communications***, Vol. 6, 6391 (2015)

8. **Jeehwan Kim***, Can Bayram*, Hongsik Park*, Cheng-Wei Cheng, Christos Dimitrakopoulos, John A. Ott, Kathleen B. Reuter, Stephen W. Bedell, and Devendra K. Sadana, "Principle of direct van der Waals epitaxy of single-crystalline films on epitaxial graphene", ***Nature Communications,*** Vol. 5, 4836 (2014)

9. **Jeehwan Kim***, Corsin Battaglia*, Mathieu Charrière, Augustin Hong, Wooshik Jung, Hongsik Park, Christophe Ballif, and Devendra Sadana, "9.4% efficient three-dimensional amorphous silicon solar cells on high aspect-ratio glass microcones", ***Advanced Materials***, Vol. 26, 4082 (2014)

10. **Jeehwan Kim*,** Homare Hiroi*, Teodor K. Todorov*, Oki Gunanwan, Masaru Kuwahara, Tayfun Gokmen, Dhruv Nair, Marinus Hopstaken, Byungha Shin, Hiroki Sugimoto, and David Mitzi, "High-efficiency $Cu_2ZnSn(S,Se)_4$ solar cells by applying a double In_2S_3/CdS emitter" ***Advanced Materials,*** Vol. 26, 7427 (2014) *Frontispiece*

11. **Jeehwan Kim***, Hongsik Park*, James B. Hannon, Stephen W. Bedell, Keith Fogel, Devendra K. Sadana, ChristosDimitrakopoulos*, "Layer-resolved graphene transfer via engineered strain layers", ***Science,*** Vol. 342, 833 (2013)

12. **Jeehwan Kim***, Augustin Hong, Bhupesh Chandra, George Tulevski, and Devendra K. Sadana, "Engineering of contact resistance between transparent single-walled carbon nanotube films and a-Si:H single junction solar cells by gold nanodots", ***Advanced Materials,*** Vol. 24, 1899 (2012)

13. **Jeehwan Kim***, Augustin J. Hong, Jae-Woong Nah, Byungha Shin, Frances M. Ross, and Devendra K. Sadana, "Three-Dimensional a-Si:H Solar Cells on Glass Nanocone Arrays Patterned by Self-Assembled Sn Nanospheres", ***ACS Nano,*** Vol. 6, 265 (2012)

14. **Jeehwan Kim***, Stephen W Bedell, and Devendra Sadana, "Multiple implantation and multiple annealing of phosphorus doped germanium to achieve n-type activation near theoretical limit" ***Applied Physics Letters,*** Vol. 101, 112107 (2012)

15. **Jeehwan Kim***, Ahmed Abou-Kandil, Augustin J. Hong, Mohamed Saad, Devendra K. Sadana, and Tze-Chiang Chen, "Efficiency Enhancement of a-Si:H single junction solar cells by a-Ge:H incorporation at the p-type a-SiC:H/transparent conducting oxide interface", ***Applied Physics Letters,*** Vol. 99, 062102 (2011)

16. **Jeehwan Kim***, Stephen W. Bedell, and Devendra K. Sadana , "Improved germanium n+/p diodes formed by coimplantation of antimony and phosphorus", ***Applied Physics Letters,*** Vol. 98, 082112 (2011)

17. **Jeehwan Kim***, Ahmed Abou-Kandil, Keith Fogel, Harold Hovel, and Devendra K Sadana "The role of high work-function metallic nanodots on the performance of a-Si:H solar cells : Offering ohmic contacts to light trapping", ***ACS Nano,*** Vol. 4, 7331 (2010)

18. **Jeehwan Kim***, Daniel Inns, Keith Fogel, and Devendra K. Sadana, "Surface texturing of single-crystalline silicon solar cells using low density SiO_2 films as an anisotropic etch mask", ***Solar Energy Materials and Solar Cells,*** Vol. 94, 2091 (2010)

19. **Jeehwan Kim***, Daniel Inns, and Devendra K. Sadana, "Investigation on critical failure thickness of hydrogenated/non-hydrogenated amorphous silicon films", ***Journal of Applied Physics,*** Vol. 107, 073507 (2010)

20. **Jeehwan Kim***, Stephen W. Bedell, Siegfried Maurer, Rainer Loesing, and Devendra K. Sadana, "Activation of implanted n-type dopants in Ge over the active concentration of 1×10^{20} cm^{-3} using co-implantation of Sb and P", ***Electrochemical and Solid-state Letters***, Vol 13, H12 (2010)

21. **Jeehwan Kim***, Daniel Inns, and Devendra K. Sadana, "Cracking behavior of evaporated amorphous silicon films", ***Thin Solid Films***, Vol. 518, 4908 (2010)

22. **Jeehwan Kim***, Stephen Bedell, Devendra Sadana, "> 10^{20} cm^{-3} n-doping in Ge by Sb/P Co-implants: n+/p Diodes with Improved Rectification", ***ECS Transactions,*** Vol 33, 201 (2010)

23. **Jeehwan Kim***, Jae Young Lee, and Ya-Hong Xie, "Fabrication of dislocation-free Si films under uniaxial tension via oxidation of porous Si substrates", ***Thin Solid Films***, Vol 516, 7599 (2008)

24. **Jeehwan Kim***, Biyun Li, and Ya-Hong Xie, "A method for fabricating dislocation-free tensile-strained SiGe films via the oxidation of porous Si substrates", ***Applied Physics Letters***, Vol 91, 252108 (2007)

25. **Jeehwan Kim*** and Ya-Hong Xie, "The fabrication of dislocation-free tensile strained Si thin films using controllably oxidized porous Si substrates", ***Applied Physics Letters***, Vol 89, 152117 (2006)

Journal Papers (Contributing-authored)

1. Piran R. Kidambi, Michael S. Boutilier, Luda Wang, Doojon Jang, **Jeehwan Kim**, and Rohit Karnik, "Selective Nanoscale Mass Transport across Atomically Thin Single Crystalline Graphene Membranes", ***Advanced Materials***, (2017)

2. Jaewoo Shim, Seo-Hyeon Jo, Minwoo Kim, Young Jae Song, **Jeehwan Kim**, and Jin-Hong Park, "Light-Triggered Ternary Device and Inverter Based on Heterojunction of van der Waals Materials", ***ACS Nano***, Vol. 11, 6319 (2017)

3. Jaewoo Shim, Hyo Seok Kim, Yoon Su Shim, Dong-Ho Kang, Hyung-Youl Park, Jaehyeong Lee, Jaeho Jeon, Seong Jun Jung, Young Jae Song, Woo-Shik Jung, Jaeho Lee, Seongjun Park, **Jeehwan Kim**, Sungjoo Lee, Yong-Hoon Kim, and Jin-Hong Park, "Extremely Large Gate Modulation in Vertical Graphene/WSe2 Heterojunction Barristor Based on a Novel Transport Mechanism", ***Advanced Materials***, Vol. 28, 5293 (2016)

4. Can Bayram, John Ott, Kuen-Ting Shiu, Cheng-Wei Cheng, Yu Zhu, **Jeehwan Kim**, Manijeh Razeghi, and Devendra Sadana, "Cubic Phase GaN on Nano-grooved Si (100) via Maskless Selective Area Epitaxy", ***Advanced Functional Materials***, Vol. 24, 4492 (2014), *Frontispiece*

5. In-yeal Lee, Hyung-Youl Park, Jin-hyung Park, Gwangwe Yoo, Myung-Hoon Lim, Junsung Park, Rathi Servin, Woo-Shik Jung, **Jeehwan Kim**, Sang-Woo Kim, Yonghan Roh, Gil-Ho Kim and Jin-Hong Park, "Poly-4-vinylphenol and Poly(melamine-co-formaldehyde)-based Graphene Passivation Method for Flexible, Wearable and Transparent Electronics", ***Nanoscale,*** Vol. 6, 3830 (2014)

6. Young T Chae, **Jeehwan Kim**, Hongsik Park, and Byungha Shin, "Building Energy Performance Evaluation of Building Integrated Photovoltaic (BIPV) Window with Semi-transparent Solar Cells", ***Applied Energy,*** Vol. 129, 217 (2014)

7. Seong-Uk Yang, Seung-Ha Choi, Jongtaek Lee, **Jeehwan Kim**, Woo-Shik Jung, Hyun-Yong Yu, Yonghan Roh, Jin-Hong Park, "Depth-Controllable Ultra Shallow Indium Gallium Zinc Oxide/Gallium Arsenide Hetero Junction Diode", ***Journal of Alloys and Compounds***, Vol. 561, 228 (2013)

8. Osama Tobail, **Jeehwan Kim**, and Devendra Sadana, "Method to Determine the Collection Length in Field-Driven a-$Si_{1-x}Ge_x$:H Solar Cells", ***Energy Procedia***, Vol. 10, 213 (2011)

9. J. Liu, T. M. Lu, **J. Kim**, K. Lai, D. C. Tsui, and Y. H. Xie, "The proximity effect of the regrowth interface on two-dimensional electron density in strained Si", ***Applied Physics Letters***, Vol 92, 112113 (2008)

10. J. Liu, **J.H. Kim**, Y.H. Xie, T.M. Lu, and K. Lai, "Epitaxial growth of two-dimensional electron gas (2DEG) in strained silicon for research on ultra-low energy electronic processes", ***Thin Solid Films***, Vol 517, 45 (2008)

11. T. M. Lu, J. Liu, **J. Kim**, K. Lai, D. C. Tsui, and Y. H. Xie, "Capacitively induced high mobility two-dimensional electron gas in undoped Si/$Si_{1-x}Ge_x$ heterostructures with atomic-layer-deposited dielectric", ***Applied Physics Letters***, Vol 90, 182114 (2007)

12. Z. M. Zhao, T. S. Yoon, W. Feng, B.Y. Li, **J. H. Kim**, J. Liu, O. Hulko, Y. H. Xie, H. M. Kim, K. B. Kim, H. J. Kim, K. L. Wang, C. Ratsch, R. Caflisch, D. Y. Ryu, and T. P. Russell, "The challenges in guided self-assembly of Ge and InAs quantum dots on Si", ***Thin Solid Films***, Vol 508, No.1, 195 (2006)

209 US Patents, Selected (122 Issued, 87 pending)

1	10,115,894	Apparatus and methods for electrical switching
2	10,056,510	Cone-shaped holes for high efficiency thin film solar cells
3	10,056,251	Hetero-integration of III-N material on silicon
4	10,043,920	Highly responsive III-V photodetectors using ZnO:Al as n-type emitter
5	10,038,057	Junction interlayer dielectric for reducing leakage current in semiconductor devices
6	10,008,625	Atomic layer deposition for photovoltaic devices
7	10,002,929	Reduction of defect induced leakage in III-V semiconductor devices
8	9,991,417	Resonant cavity strained III-V photodetector and LED on silicon substrate
9	9,991,113	Systems and methods for fabricating single-crystalline diamond membranes
10	9,960,830	Method and apparatus for managing beam in beamforming system
11	9,947,533	Selective epitaxy using epitaxy-prevention layers
12	9,947,529	Porous fin as compliant medium to form dislocation-free heteroepitaxial films
13	9,935,215	Transparent conductive electrode for three dimensional photovoltaic device
14	9,929,060	Porous silicon relaxation medium for dislocation free CMOS devices
15	9,917,220	Buffer layer for high performing and low light degraded solar cells
16	9,917,215	Double layered transparent conductive oxide for reduced schottky barrier in photovoltaic devices
17	9,917,021	Porous silicon relaxation medium for dislocation free CMOS devices
18	9,916,984	Self-aligned source and drain regions for semiconductor devices
19	9,911,888	Photovoltaic device having layer with varying crystallinity
20	9,905,637	Reduction of defect induced leakage in III-V semiconductor devices
21	9,887,265	MOSFET with ultra low drain leakage
22	9,876,129	Cone-shaped holes for high efficiency thin film solar cells
23	9,865,520	Tunable semiconductor band gap reduction by strained sidewall passivation
24	9,865,509	FinFET CMOS with Si NFET and SiGe PFET
25	9,818,909	LED light extraction enhancement enabled using self-assembled particles patterned surface
26	9,818,901	Wafer bonded solar cells and fabrication methods
27	9,806,211	Tandem solar cell with improved absorption material
28	9,799,792	Substrate-free thin-film flexible photovoltaic device and fabrication method
29	9,799,747	Low resistance contact for semiconductor devices
30	9,786,756	Self-aligned source and drain regions for semiconductor devices
31	9,768,254	Leakage-free implantation-free ETSOI transistors
32	9,748,412	Highly responsive III-V photodetectors using ZnO:Al as N-type emitter
33	9,741,890	Protective insulating layer and chemical mechanical polishing for polycrystalline thin film solar cells
34	9,741,880	Three-dimensional conductive electrode for solar cell
35	9,722,120	Bandgap grading of CZTS solar cell
36	9,722,033	Doped zinc oxide as n+ layer for semiconductor devices
37	9,716,207	Low reflection electrode for photovoltaic devices
38	9,716,195	Dry etch method for texturing silicon and device
39	9,712,296	Hybrid zero-forcing beamforming method and apparatus
40	9,705,575	Advanced feedback and reference signal transmissions for MIMO wireless communication systems
41	9,691,847	Self-formation of high-density arrays of nanostructures
42	9,673,290	Self-aligned source and drain regions for semiconductor devices
43	9,666,674	Formation of large scale single crystalline graphene
44	9,660,116	Nanowires formed by employing solder nanodots
45	9,653,570	Junction interlayer dielectric for reducing leakage current in semiconductor devices
46	9,646,832	Porous fin as compliant medium to form dislocation-free heteroepitaxial films
47	9,634,164	Reduced light degradation due to low power deposition of buffer layer

48 9,620,592 Doped zinc oxide and n-doping to reduce junction leakage

49 9,607,952 High-z oxide nanoparticles embedded in semiconductor package

50 9,601,583 Hetero-integration of III-N material on silicon

51 9,583,562 Reduction of defect induced leakage in III-V semiconductor devices

52 9,577,196 Optoelectronics integration by transfer process

53 9,574,287 Gallium nitride material and device deposition on graphene terminated wafer and method of forming the same

54 9,559,120 Porous silicon relaxation medium for dislocation free CMOS devices

55 9,537,038 Solar cell made using a barrier layer between P-type and intrinsic layers

56 9,536,945 MOSFET with ultra low drain leakage

57 9,530,643 Selective epitaxy using epitaxy-prevention layers

58 9,515,215 Efficiency restoration in a photovoltaic cell

59 9,490,455 LED light extraction enhancement enabled using self-assembled particles patterned surface

60 9,484,347 FinFET CMOS with Si NFET and SiGe PFET

61 9,459,797 Uniformly distributed self-assembled cone-shaped pillars for high efficiency solar cells

62 9,443,997 Hybrid CZTSSe photovoltaic device

63 9,443,957 Self-aligned source and drain regions for semiconductor devices

64 9,418,870 Silicon germanium-on-insulator formation by thermal mixing

65 9,401,397 Reduction of defect induced leakage in III-V semiconductor devices

66 9,394,178 Wafer scale epitaxial graphene transfer

67 9,379,259 Double layered transparent conductive oxide for reduced schottky barrier in photovoltaic devices

68 9,337,436 Transferable transparent conductive oxide

69 9,337,274 Formation of large scale single crystalline graphene

70 9,331,220 Three-dimensional conductive electrode for solar cell

71 9,324,813 Doped zinc oxide as N.sup.+ layer for semiconductor devices

72 9,324,794 Self-formation of high-density arrays of nanostructures

73 9,324,566 Controlled spalling using a reactive material stack

74 9,318,641 Nanowires formed by employing solder nanodots

75 9,312,132 Method of forming high-density arrays of nanostructures

76 9,306,107 Buffer layer for high performing and low light degraded solar cells

77 9,231,133 Nanowires formed by employing solder nanodots

78 9,214,577 Reduced light degradation due to low power deposition of buffer layer

79 9,203,022 Resistive random access memory devices with extremely reactive contacts

80 9,190,549 Solar cell made using a barrier layer between p-type and intrinsic layers

81 9,153,729 Atomic layer deposition for photovoltaic devices

82 9,123,842 Photoreceptor with improved blocking layer

83 9,123,838 Transparent conductive electrode for three dimensional photovoltaic device

84 9,105,854 Transferable transparent conductive oxide

85 9,105,805 Enhancing efficiency in solar cells by adjusting deposition power

86 9,099,664 Transferable transparent conductive oxide

87 9,096,050 Wafer scale epitaxial graphene transfer

88 9,093,290 Self-formation of high-density arrays of nanostructures

89 9,070,617 Reduced S/D contact resistance of III-V mosfet using low temperature metal-induced crystallization of n+ Ge

90 9,059,272 Self-aligned III-V MOSFET fabrication with in-situ III-V epitaxy and in-situ metal epitaxy and contact formation

91 9,059,271 Self-aligned III-V MOSFET fabrication with in-situ III-V epitaxy and in-situ metal epitaxy and contact formation

92 9,059,013 Self-formation of high-density arrays of nanostructures
93 9,040,428 Formation of metal nanospheres and microspheres
94 9,040,340 Temperature grading for band gap engineering of photovoltaic devices
95 9,035,282 Formation of large scale single crystalline graphene
96 8,933,456 Germanium-containing release layer for transfer of a silicon layer to a substrate
97 8,927,857 Silicon: hydrogen photovoltaic devices, such as solar cells, having reduced light induced degradation and method of making such devices
98 8,916,451 Thin film wafer transfer and structure for electronic devices
99 8,916,409 Photovoltaic device using nano-spheres for textured electrodes
100 8,901,695 High efficiency solar cells fabricated by inexpensive PECVD

Invited Talks

1. **Nature** London headquarter office, “Nanoelectronics Group at MIT” 2018
2. **LDMO** “Manufacturing of wafer-scale freestanding 3D and 2D materials with atomic precision control”, Shenzhen, China 2018
3. **University of Michigan** “Material challenges and opportunities in next generation electronics”, 2018
4. **Michigan State University** “Material challenges and opportunities in next generation electronics”, 2018
5. **Stanford University** “New Paradigm of Resistive Memory that can Enable Large-Scale Neuromorphic Computing” 2018
6. **University of California, Berkeley** “III-V epitaxy for low energy optoelectronics”, 2018
7. **Stevens Institute of Technology** “Material challenges and opportunities in next generation electronics” 2018
8. **ETRI**, Korea “Material challenges and opportunities in next generation electronics” 2018
9. **KAIST** “Material challenges and opportunities in next generation electronics” 2018
10. **SKKU** “Material challenges and opportunities in next generation electronics” 2018
11. **Amore Pacific**, “Ultrasensitive electronic skin sensor system” 2018
12. **Samsung Electronics** “New Paradigm of Resistive Memory that can Enable Large-Scale Neuromorphic Computing” 2018
13. **ICFO**, Barcelona, Spain, “2D material-based layer transfer and its applications for wafer-scale 2D/3D heterostructures”, 2018
14. **UKC**, New York “New paradigm of resistive memory that can enable large-scale neuromorphic computing”, Shenzhen, China, 2018
15. **Gordon Conference** “2D Heterostructure Assembly”, Massachusetts, MA, 2018
16. **Harvard University** “Material challenges and opportunities in next generation electronics: From non-silicon electronics to artificial neural network”, 2018
17. **Hong Kong Polytechnic University** “Material challenges and opportunities in next generation electronics: From non-silicon electronics to artificial neural network”, 2018
18. **Huawei** “New paradigm of resistive memory that can enable large-scale neuromorphic computing”, Shenzhen, China, 2018
19. **IUMRS (Plenary)**, Korea “New Paradigm of Resistive Memory that can Enable Large-Scale Neuromorphic Computing” 2018
20. **GPVC (Plenary)**, Korea “New strategy for recycling wafers: 2D material-based layer transfer (2DLT)” 2018
21. **Boston University** “Material challenges and opportunities in next generation electronics: From non-silicon electronics to artificial neural network”, 2018
22. **Naval Research Laboratory** “Material challenges and opportunities in next generation electronics: From non-silicon electronics to artificial neural network”, 2018
23. **Lawrence Epitaxy conference** “Material challenges and opportunities in next generation electronics” 2018
24. **MRS Fall** “Uniform epitaxial SiGe memory by one dimensional filament confinement for large-scale synaptic arrays”, Boston, 2017
25. **MIT Mechanical Engineering Colloquium**, “Material challenges and opportunities in next generation electronics: From non-silicon electronics to artificial neural network”, 2017
26. **Hynix** “New paradigm of resistive memory that can enable large-scale neuromorphic computing”, Ichon, Korea, 2018
27. **Tsinghua University** “2D material-based layer transfer based on remote epitaxy & uniform epitaxial RAM towards large-scale neuromorphic arrays”, 2017
28. **University of California, Berkeley** “2D material-based layer transfer based on remote epitaxy & uniform epitaxial RAM towards large-scale neuromorphic arrays”, 2017
29. **Stanford University** “2D material-based layer transfer based on remote epitaxy & uniform epitaxial RAM towards large-scale neuromorphic arrays”, 2017

30. **University of California, Santa Barbara** “2D material-based layer transfer based on remote epitaxy & uniform epitaxial RAM towards large-scale neuromorphic arrays”, 2017
31. **University of Illinois, Urbana-Champaign** “2D material-based layer transfer based on remote epitaxy & uniform epitaxial RAM towards large-scale neuromorphic arrays”, 2017
32. **University of Massachusetts, Amherst** “Innovation in epitaxy still required for next generation computing”, 2017
33. **2D Electronic Materials Symposium** “Remote epitaxy through graphene” Santa Fe, NM, 2017
34. “Recent Advance in graphene-based layer transfer”, **ECS**, New Orleans, LA, 2017
35. “Recent Advance in graphene-based layer transfer”, **TMS**, San Diego, CA, 2017
36. “Graphene-based layer transfer”, **Semicon Korea**, Seoul, 2017
37. “Extremely cost-effective semiconductor layer transfer & Advanced epitaxial RAM”, **MIT-Japan conference**, Tokyo, 2017
38. “Recent Advance in graphene-based layer transfer”, **MRS** Fall, Boston, 2016
39. “Advanced ReRAM for neuromorphic computing”, **Samsung**, Seoul, Korea, 2016
40. “Nanoelectronics Group at MIT”, **Seoul National University**, Seoul, Korea, 2016
41. “Nanoelectronics Group at MIT”, **KAIST**, Daejon, Korea, 2016
42. “Nanoelectronics Group at MIT”, **Hynix**, Ichon, Korea, 2016
43. “Graphene-based layer transfer for low-cost, high-throughput, high-efficiency solar cells”, **LG Electronics**, Seoul, Korea, 2015
44. “Single-crystalline graphene and its application for semiconductor layer transfers”, **Lincoln Laboratory**, 2015
45. “Single-crystalline graphene and its application for semiconductor layer transfers”, **NASA Jet Propulsion Laboratory**, Los Angeles, 2015
46. “Single-crystalline graphene and its application for semiconductor layer transfers, **SKKU**, Seoul, Korea, 2015
47. “Nanotechnology for Photovoltaics: Strategies for scalable manufacturing of efficient solar cells”, Energy Science Institute, **Yale University**, 2015
48. "Atomic-precision control of nanoscale materials via strain engineering towards scalable manufacturing", Mechanical Engineering, **MIT**, 2015
49. "Material innovations for nanoelectronics: Atomic-precision control of two-dimensional materials", School of Engineering and Applied Science, **Harvard University**, 2015
50. "Atomic-Precision Control of Single-Crystalline 2D Materials & Design Principles of 3D PV Architectures", Electrical and Computer Engineering , **University of Illinois, Urbana-Champaign**, 2014
51. “Atomic-precision Control of Single-crystalline 2D Materials & Recent Progress on Thin Film PV in IBM”, Electrical Engineering, **UC Berkeley**, 2014
52. “Atomic-precision Control of Single-crystalline 2D Materials & Recent Progress on Thin Film PV in IBM”, Yale Institute for Nanoscience and Quantum Engineering, **Yale University**, 2014
53. “Wafer-scale Single-crystalline Graphene & High-aspect Ratio Three-dimensional PV”, Applied Physics and Materials Science, **Caltech**, 2014
54. “Wafer-scale Single-crystalline Graphene and Its applications”, Department of Materials Science and Engineering, **UCLA**, 2014
55. “Atomic-precision Control of Two-dimensional Materials & Design Principles of Three-dimensional PV Architectures”, Materials Department, **UC Santa Barbara**, 2014
56. “Atomic-precision Control of Two-dimensional Materials & Design Principles of Three-dimensional PV Architectures”, Department of Materials Science and Engineering, **MIT**, 2014
57. “Nanocone-based three dimensional thin film silicon solar cells” **SPIE**, San Diego, CA, 2012
58. “Nanostructured 3D Solar cells”, Department of Materials Science and Engineering, **UCLA**, 2012
59. “Nanocone-based three dimensional thin film silicon solar cells”, Department of Electrical Engineering, **Sungkyunkwan University**, Korea, 2012
60. “Role of Nanostructures on the Performance of a-Si:H Solar Cells”, **Optical Society of America**, Austin, TX, 2011
61. “Effect of Work-Function Engineering of p+/TCO interface on the Performance of a-Si:H Solar Cell”, IMT, **École Polytechnique Fédérale de Lausanne (EPFL)**, Switzerland, 2011
62. “The role of high work-function metallic nanodots on the performance of amorphous silicon solar cells”, Department of Materials Science and Engineering, **Seoul National University**, Korea, 2010
63. “Plasmonics in thin film solar cells”, Department of Electrical Engineering, **KAIST**, Korea, 2010
64. Solar cell and Advanced CMOS research in IBM”, Department of Materials Science and Engineering, **UCLA**, 2010
65. “Plasmonics in thin film solar cells”, Department of Materials Science & Engineering, **Hongik University**, Korea, 2010
66. "n-type Ge MOSFET”, **Korea Advanced Nano Fabrication Center**, Korea, 2010